

# MC100LVEP14

## 2.5V / 3.3V 1:5 Differential ECL/PECL/HSTL Clock Driver

### Description

The MC100LVEP14 is a low skew 1-to-5 differential driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The ECL/PECL input signals can be either differential or single-ended (if the  $V_{BB}$  output is used). HSTL inputs can be used when the LVEP14 is operating under PECL conditions.

The LVEP14 specifically guarantees low output-to-output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

To ensure that the tight skew specification is realized, both sides of any differential output need to be terminated identically into 50  $\Omega$  even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

The common enable ( $\overline{EN}$ ) is synchronous, outputs are enabled/disabled in the LOW state. This avoids a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock; therefore, all associated specification limits are referenced to the negative edge of the clock input.

The MC100LVEP14, as with most other ECL devices, can be operated from a positive  $V_{CC}$  supply in PECL mode. This allows the LVEP14 to be used for high performance clock distribution in +3.3 V or +2.5 V systems. Single-ended CLK input pin operation is limited to a  $V_{CC} \geq 3.0$  V in PECL mode, or  $V_{EE} \leq -3.0$  V in NECL mode. Designers can take advantage of the LVEP14's performance to distribute low skew clocks across the backplane or the board.

### Features

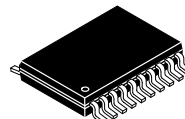
- 100 ps Device-to-Device Skew
- 25 ps Within Device Skew
- 400 ps Typical Propagation Delay
- Maximum Frequency > 2 GHz Typical
- The 100 Series Contains Temperature Compensation
- PECL and HSTL Mode:  
 $V_{CC} = 2.375$  V to 3.8 V with  $V_{EE} = 0$  V
- NECL Mode:  
 $V_{CC} = 0$  V with  $V_{EE} = -2.375$  V to -3.8 V
- LVDS Input Compatible
- Open Input Default State
- Pb-Free Packages are Available\*

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



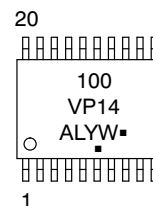
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<http://onsemi.com>



TSSOP-20  
DT SUFFIX  
CASE 948E

### MARKING DIAGRAM\*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

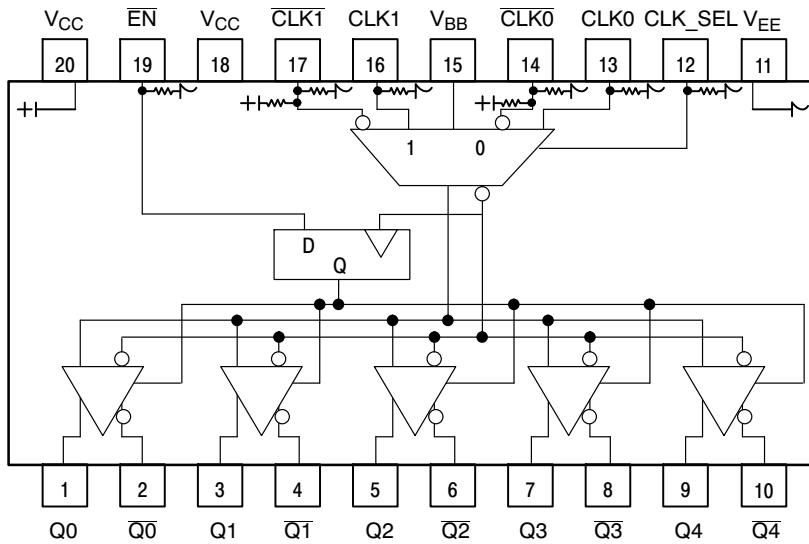
(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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Warning: All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. 20-Lead Pinout (Top View) and Logic Diagram**

**Table 1. PIN DESCRIPTION**

Pin	Type	Function
CLK0*, CLK0**	LVECL/LVPECL/HSTL	ECL/PECL/HSTL CLK Input
CLK1*, CLK1**	LVECL/LVPECL/HSTL	ECL/PECL/HSTL CLK Input
Q0:4, Q0:4	LVECL/LVPECL	ECL/PECL Outputs
CLK_SEL*	LVECL/LVPECL	ECL/PECL Active Clock Select Input
EN*	LVECL/LVPECL	ECL Sync Enable
V <sub>BB</sub>	LVECL/LVPECL	Reference Voltage Output
V <sub>CC</sub>		Positive Supply
V <sub>EE</sub>		Negative Supply

\* Pins will default low when left open.

\*\*Pins will default to  $V_{CC}/2$  when left open.

**Table 2. FUNCTION TABLE**

CLK0	CLK1	CLK_SEL	EN	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

\*On next negative transition of CLK0 or CLK1

**Table 3. ATTRIBUTES**

Characteristics	Value	
Internal Input Pulldown Resistor	75 k $\Omega$	
Internal Input Pullup Resistor	37.5 k $\Omega$	
ESD Protection	Human Body Model	> 2 kV
	Machine Model	> 100 V
	Charged Device Model	> 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb Pkg	Pb-Free Pkg
	TSSOP-20	Level 1
		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	357 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

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**Table 4. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		6	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		-6	V
V <sub>I</sub>	PECL Mode Input Voltage	V <sub>EE</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub>	6	V
	NECL Mode Input Voltage	V <sub>CC</sub> = 0 V	V <sub>I</sub> ≥ V <sub>EE</sub>	-6	V
I <sub>out</sub>	Output Current	Continuous Surge		50	mA
				100	mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			± 0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm	TSSOP-20	140	°C/W
		500 lfpm	TSSOP-20	100	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-20	23 to 41	°C/W
T <sub>sol</sub>	Wave Solder	Pb Pb-Free		265	°C
				265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 5. 100LVEP DC CHARACTERISTICS, PECL V<sub>CC</sub> = 2.5 V, V<sub>EE</sub> = 0 V (Note 2)**

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current	45	60	75	45	60	75	45	60	75	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 3)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V <sub>OL</sub>	Output LOW Voltage (Note 3)	555	730	900	555	730	900	555	730	900	mV
V <sub>IH</sub>	Input HIGH Voltage (Single-Ended) (Note 4)	1335		1620	1335		1620	1275		1620	mV
V <sub>IL</sub>	Input LOW Voltage (Single-Ended) (Note 4)	555		900	555		900	555		900	mV
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 5)	1.2		2.5	1.2		2.5	1.2		2.5	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	CLK	0.5		0.5			0.5			μA
		CLK	-150		-150			-150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.125 V to -1.3 V.
- All loading with 50 Ω to V<sub>CC</sub> - 2.0 V.
- Do not use V<sub>BB</sub> at V<sub>CC</sub> < 3.0 V.
- V<sub>IHCMR</sub> min varies 1:1 with V<sub>EE</sub>; V<sub>IHCMR</sub> max varies 1:1 with V<sub>CC</sub>. The V<sub>IHCMR</sub> range is referenced to the most positive side of the differential input signal.

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**Table 6. 100LVEP DC CHARACTERISTICS, PECL**  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 6)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	45	60	75	45	60	75	45	60	75	mA
$V_{OH}$	Output HIGH Voltage (Note 7)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
$V_{OL}$	Output LOW Voltage (Note 7)	1355	1530	1700	1355	1530	1700	1355	1530	1700	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1355		1700	1355		1700	1355		1700	mV
$V_{BB}$	Output Reference Voltage (Note 8)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9)	1.2		3.3	1.2		3.3	1.2		3.3	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	CLK CLK	0.5 -150		0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.925 V to -0.5 V.
7. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .
8. Single-ended input operation is limited to  $V_{CC} \geq 3.0\text{ V}$  in PECL mode.
9.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 7. 100LVEP DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -3.8\text{ V}$  to  $-2.375\text{ V}$  (Note 10)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	45	60	75	45	60	75	45	60	95	mA
$V_{OH}$	Output HIGH Voltage (Note 11)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
$V_{OL}$	Output LOW Voltage (Note 11)	-1945	-1770	-1600	-1945	-1770	-1600	-1945	-1770	-1600	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1945		-1600	-1945		-1600	-1945		-1600	mV
$V_{BB}$	Output Reference Voltage (Note 12)	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13)	$V_{EE} + 1.2$		0.0	$V_{EE} + 1.2$		0.0	$V_{EE} + 1.2$		0.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	CLK CLK	0.5 -150		0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. Input and output parameters vary 1:1 with  $V_{CC}$ .
11. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .
12. Single-ended input operation is limited to  $V_{EE} \leq 3.0\text{ V}$  in NECL mode.
13.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 8. DC CHARACTERISTICS, HSTL**  $V_{CC} = 2.375\text{ V to }3.8\text{ V}$ ,  $V_{EE} = 0\text{ V}$

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{IH}$	Input HIGH Voltage	1200			1200			1200			mV
$V_{IL}$	Input LOW Voltage			400			400			400	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

**Table 9. AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -2.375\text{ V to }-3.8\text{ V}$  or  $V_{CC} = 2.375\text{ V to }3.8\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 14)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OUTPP}$	Output Voltage Amplitude @ 2.5 GHz (Figure 2)	330	425		280	375		230	295		mV
$t_{PLH}$ $t_{PHL}$	Propagation Delay to Output Differential	300	375	425	300	400	475	300	430	525	ps
$t_{skew}$	Within-Device Skew (Note 15) Device-to-Device Skew (Note 15)		10 100	25 125		15 150	25 175		15 200	25 225	ps
$t_s$ $t_h$	Setup Time Hold Time	EN EN	100 200	50 140	100 200	50 140		100 200	50 140		ps
$t_{JITTER}$	CLOCK Random Jitter (RMS) @ $\leq 1.0\text{ GHz}$ @ $\leq 1.5\text{ GHz}$ @ $\leq 2.0\text{ GHz}$ @ $\leq 2.5\text{ GHz}$		0.157 0.163 0.180 0.179	0.3 0.2 0.3 0.3		0.181 0.176 0.201 0.208	0.3 0.3 0.3 0.3		0.212 0.218 0.235 0.253	0.3 0.3 0.3 0.4	ps
$V_{PP}$	Minimum Input Swing	150	800	1200	150	800	1200	150	800	1200	mV
$t_r/t_f$	Output Rise/Fall Time (20%–80%)	125	165	225	125	180	250	125	200	275	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

14. Measured using a 750 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

15. Skew is measured between outputs under identical transitions.

## Resource Reference of Application Notes

- AN1405/D** - ECL Clock Distribution Techniques
- AN1406/D** - Designing with PECL (ECL at +5.0 V)
- AN1503/D** - ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** - Metastability and the ECLinPS Family
- AN1568/D** - Interfacing Between LVDS and ECL
- AN1672/D** - The ECL Translator Guide
- AND8001/D** - Odd Number Counters Design
- AND8002/D** - Marking and Date Codes
- AND8020/D** - Termination of ECL Logic Devices
- AND8066/D** - Interfacing with ECLinPS
- AND8090/D** - AC Characteristics of ECL Devices

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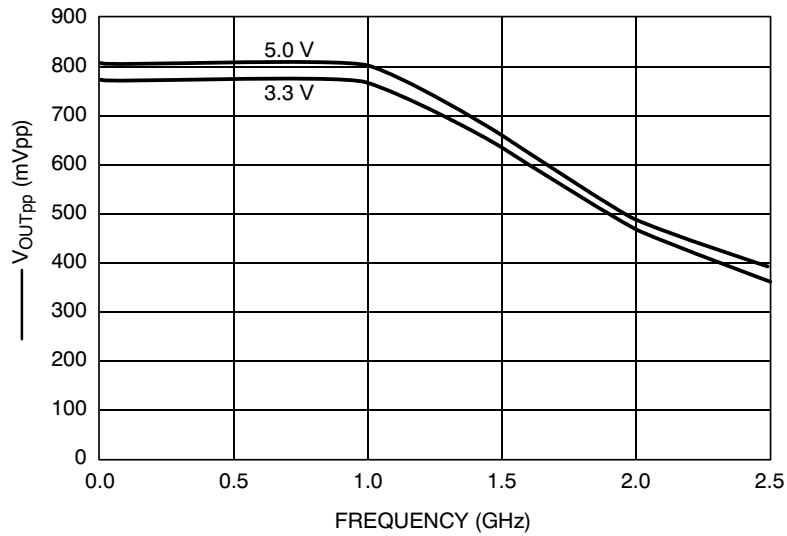


Figure 2. Typical V<sub>OUTTPP</sub> (mVpp) versus Frequency (GHz) @ 25°C

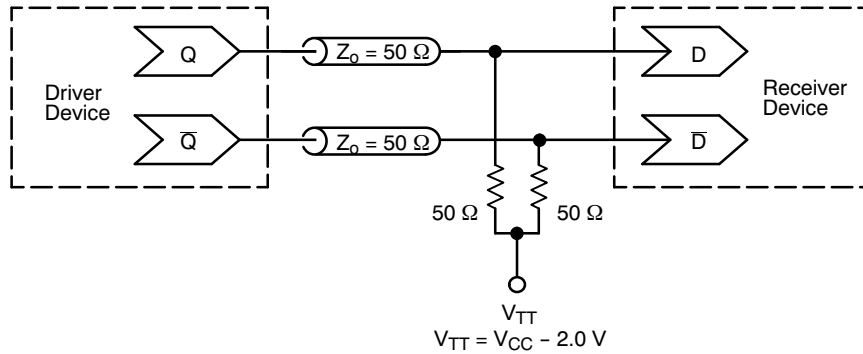


Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC100LVEP14DT	TSSOP-20*	75 Units / Rail
MC100LVEP14DTG	TSSOP-20*	75 Units / Rail
MC100LVEP14DTR2	TSSOP-20*	2500 / Tape & Reel
MC100LVEP14DTR2G	TSSOP-20*	2500 / Tape & Reel

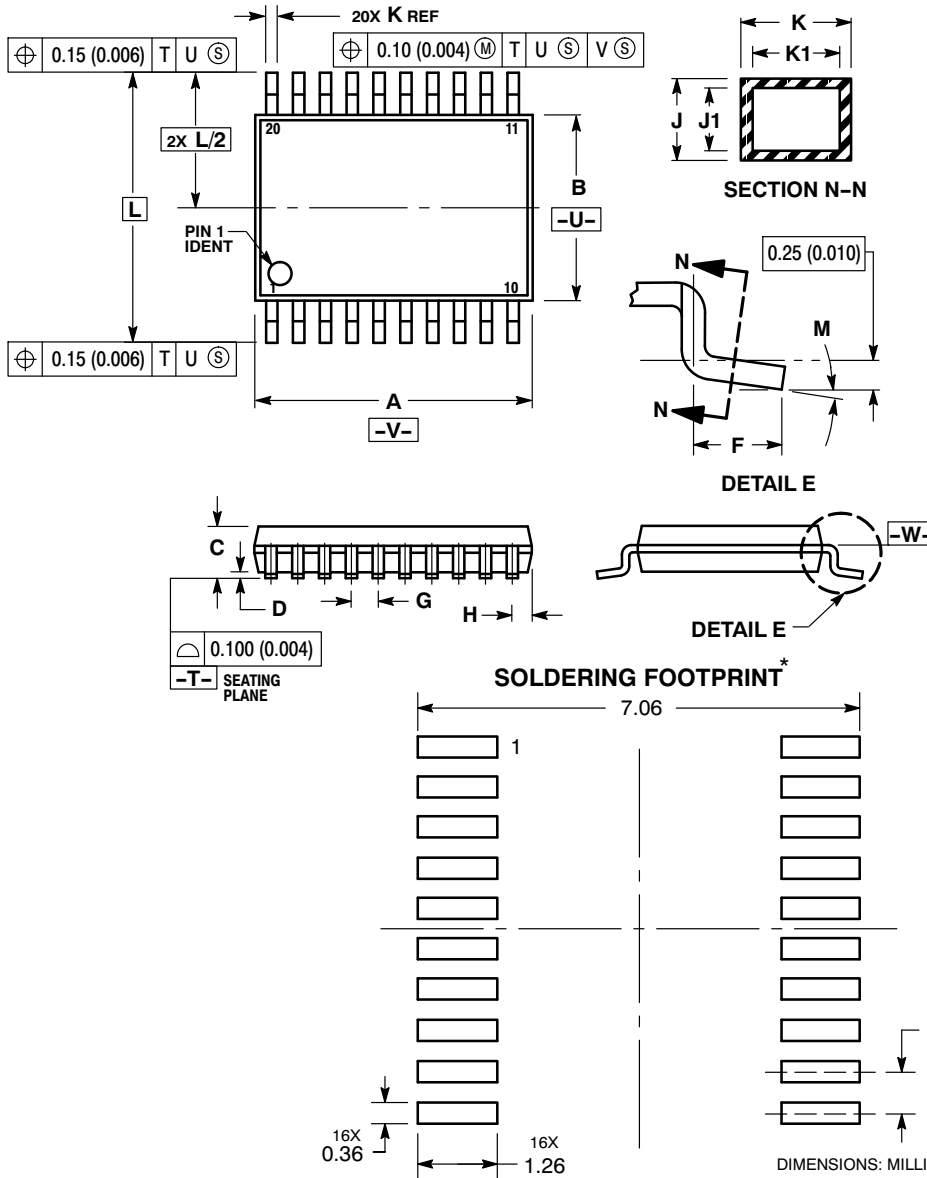
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

# MC100LVEP14

## PACKAGE DIMENSIONS

TSSOP-20  
CASE 948E-02  
ISSUE C



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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